DATA SHEET

74ALVT162823

18-bit bus-interface D-type flip-flop
with reset and enable
with 30Ω termination resistors (3-State)

Product specification

1998 Aug 27

IC24 Data Handbook

Philips
Semiconductors

PHILIPS

2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

74ALVT162823

FEATURES

- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- 5V I/O Compatible
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up Reset
- Output capability: +12mA/–12mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Outputs include series resistance of 30Ω making external termination resistors unnecessary

DESCRIPTION

The 74ALVT162823 18-bit bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ALVT162823 has two 9-bit wide buffered registers with Clock Enable ($n\overline{CE}$) and Master Reset ($n\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 74ALVT162823 is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF	4.2 3.4	3.0 2.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	3	pF
C_{OUT}	Output capacitance	$V_{I/O}$ = 0V or 3.0V	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT162823 DL	AV162823 DL	SOT371–1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT162823 DGG	AV162823 DGG	SOT364–1

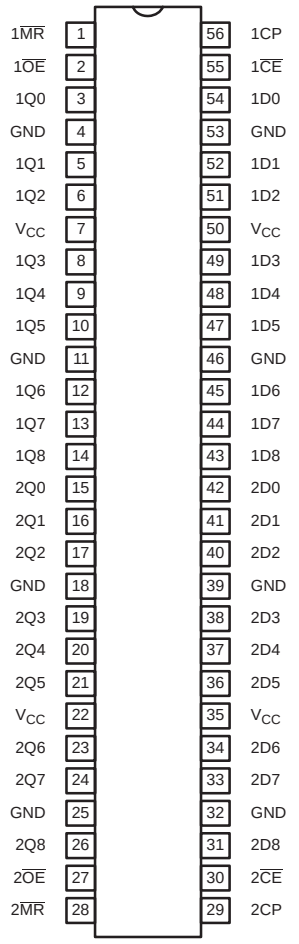
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
2, 27	$1\overline{OE}$, $2\overline{OE}$	Output enable input (active-Low)
54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31	1D0-1D8 2D0-2D8	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26	1Q0-1Q8 2Q0-2Q8	Data outputs
56, 29	1CP, 2CP	Clock pulse input (active rising edge)
55, 30	$1\overline{CE}$, $2\overline{CE}$	Clock enable input (active-Low)
1, 28	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

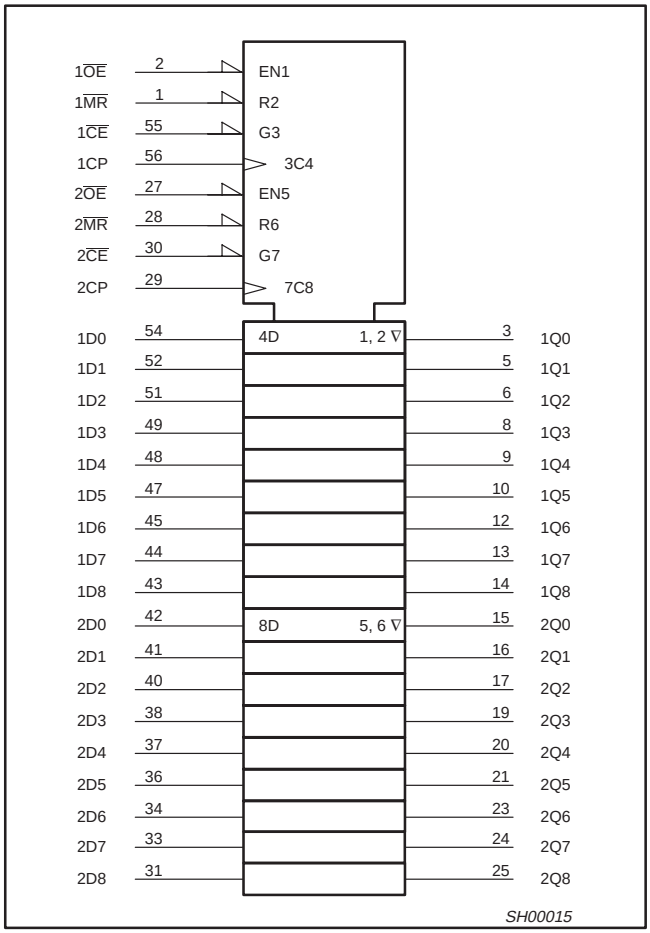
74ALVT162823

PIN CONFIGURATION



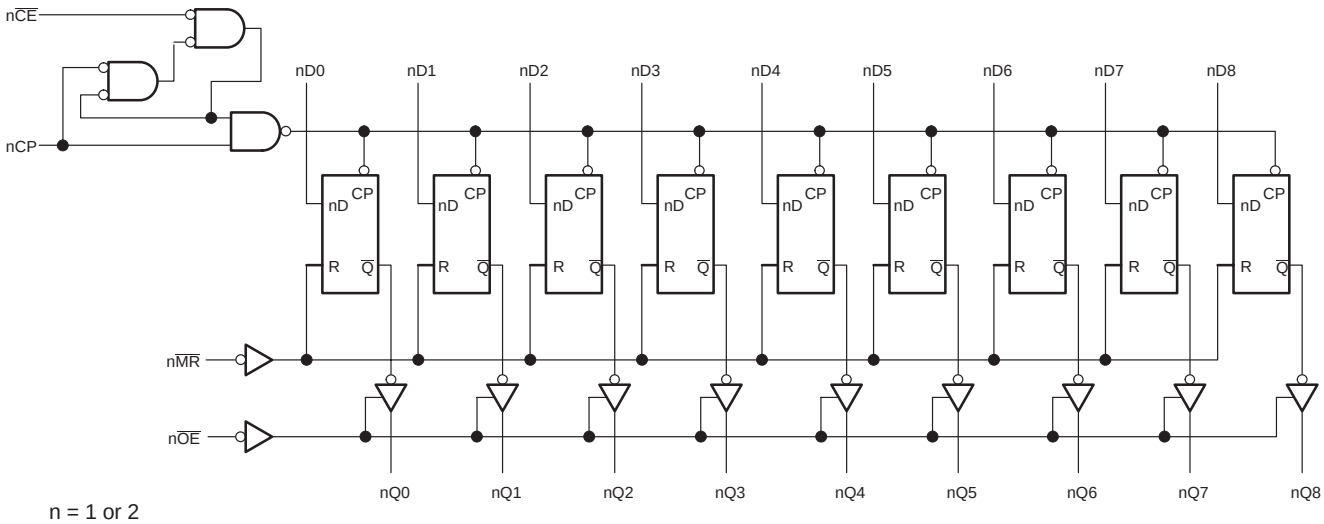
SH00014

LOGIC SYMBOL (IEEE/IEC)



SH00015

LOGIC DIAGRAM



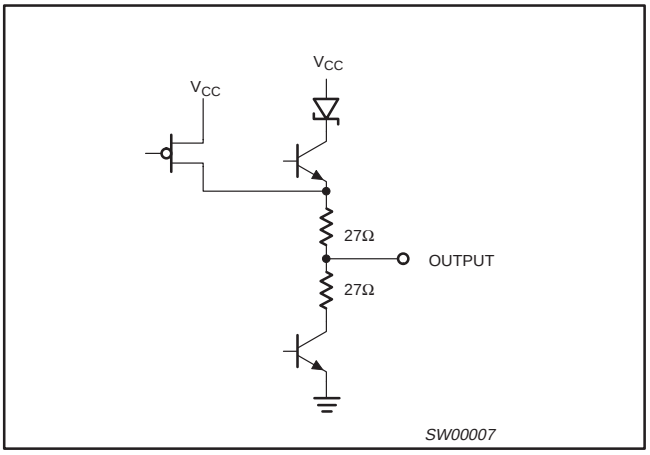
SH00016

FUNCTION TABLE

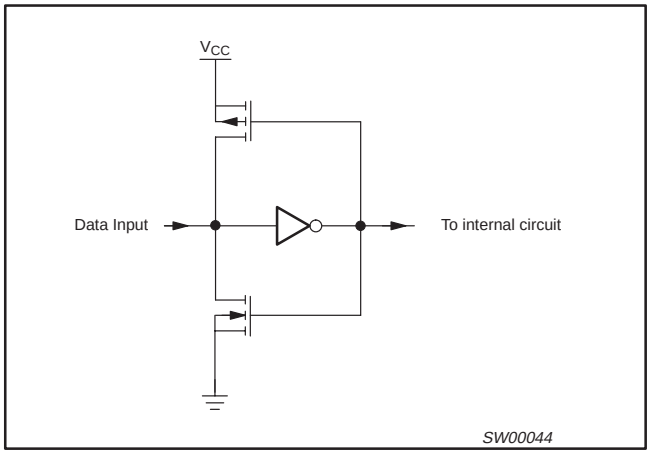
INPUTS					OUTPUTS	OPERATING MODE
$n\overline{OE}$	$n\overline{MR}$	$n\overline{CE}$	nCP	nDx	nQ0 – nQ8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↕	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

SCHEMATIC OF EACH OUTPUT



BUS HOLD CIRCUIT



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = –12mA		2.0	2.3		V
V_{OL}	Low-level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA			0.5	0.8	V
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V	Control pins		0.1	10	µA
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]		0.1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	µA
		V_{CC} = 3.6V; V_I = 0	Data pins[4]		0.1	-5	µA
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current D inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		µA
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq 1.2V$; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.05	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.9	5.5	mA
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = –40°C to +85°C V_{CC} = +3.3V ±0.3V			
			MIN	TYP	MAX	
f_{MAX}	Maximum clock frequency	1				MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.8 1.8	3.0 2.8	4.7 4.0	ns
t_{PHL}	Propagation delay n$\overline{MR}$ to nQx	2	1.8	2.8	4.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.9 1.6	3.5 2.6	5.7 3.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.9 1.5	3.4 2.5	5.2 3.8	ns

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			T_{amb} = -40 to +85°C V_{CC} = +3.3V ±0.3V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time, High or Low nDx to nCP	3	1.0 1.2	0.6 0.7	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nCP	3	0.1 0.1	–0.8 –0.6	ns
t_w(H) t_w(L)	nCP pulse width High or Low	1	1.5 2.5	0.7 1.7	ns
t_s(H) t_s(L)	Setup time, High or Low n$\overline{CE}$ to nCP	3	1.0 0.5	0.2 –0.5	ns
t_h(H) t_h(L)	Hold time, High or Low n$\overline{CE}$ to nCP	3	1.0 1.0	0.5 –0.1	ns
t_w(L)	n$\overline{MR}$ pulse width, Low	2	2.0	1.5	ns
t_{rec}	Recovery time n$\overline{MR}$ to nCP	2	2.0	1.4	ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3V; I_{OH} = –8mA		1.7	2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 12mA			0.3	0.5	V
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND			0.2	0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = GND	Control pins		0.1	±1	µA
		V_{CC} = 2.7V; V_I = 5.5V	Control pins		0.1	10	µA
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]		0.1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	µA
		V_{CC} = 3.6V; V_I = 0	Data pins[4]		0.1	-5	µA
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current D inputs[6]	V_{CC} = 2.5V; V_I = 0.7V			100		µA
		V_{CC} = 2.5V; V_I = 1.7V			–70		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.5V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.7	4.5	mA
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = –40°C to +85°C V_{CC} = +2.5V ±0.2V			
			MIN	TYP	MAX	
f_{MAX}	Maximum clock frequency	1				MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	2.5 2.0	4.2 3.4	6.3 5.0	ns
t_{PHL}	Propagation delay n$\overline{MR}$ to nQx	2	2.0	3.4	4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	3.0 2.0	4.8 3.2	7.6 5.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	2.5 2.0	4.4 3.3	6.7 5.2	ns

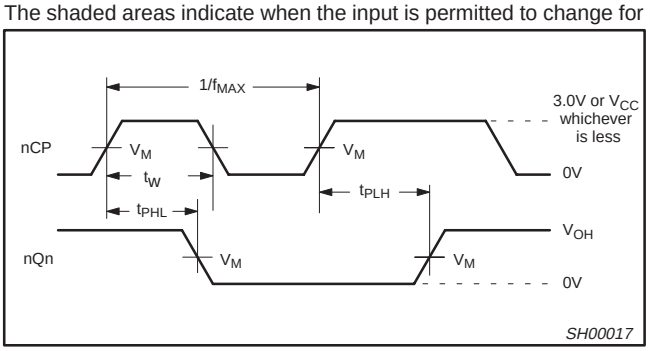
AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

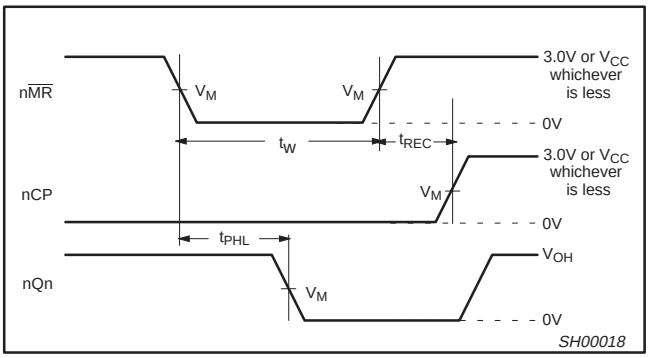
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			T_{amb} = -40 to +85°C V_{CC} = +2.5V ±0.2V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time, High or Low nDx to nCP	3	1.0 2.0	0.6 1.4	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nCP	3	0.1 0.1	–1.5 –0.6	ns
t_w(H) t_w(L)	nCP pulse width High or Low	1	2.0 3.0	0.8 2.1	ns
t_s(H) t_s(L)	Setup time, High or Low n$\overline{CE}$ to nCP	3	1.0 0.5	0.2 –0.2	ns
t_h(H) t_h(L)	Hold time, High or Low n$\overline{CE}$ to nCP	3	1.0 1.0	0.2 –0.1	ns
t_w(L)	n$\overline{MR}$ pulse width, Low	2	2.5	1.6	ns
t_{rec}	Recovery time n$\overline{MR}$ to nCP	2	2.3	1.7	ns

AC WAVEFORMS

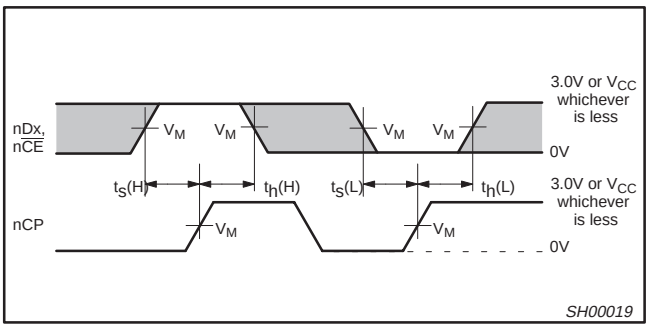
For all waveforms, V_M = 1.5V or V_{CC}/2 whichever is less
The shaded areas indicate when the input is permitted to change for predictable output performance.



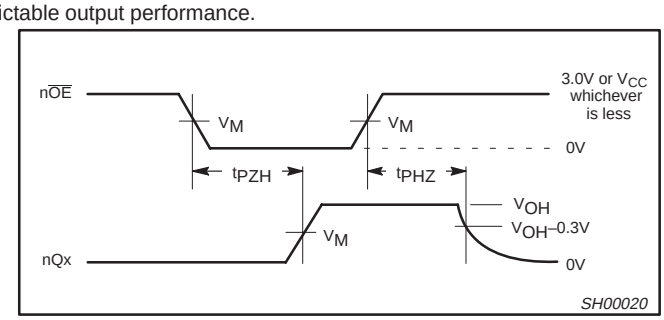
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



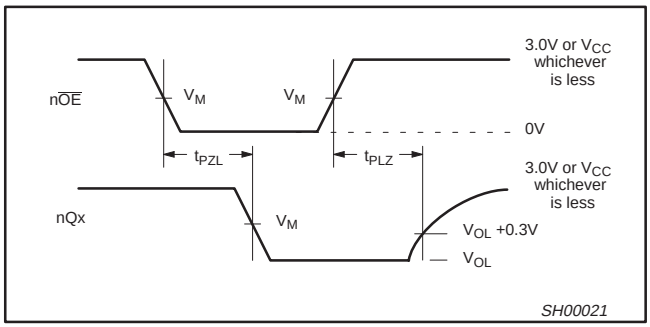
Waveform 2. Master Reset Pulse WIdth, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Data Setup and Hold Times

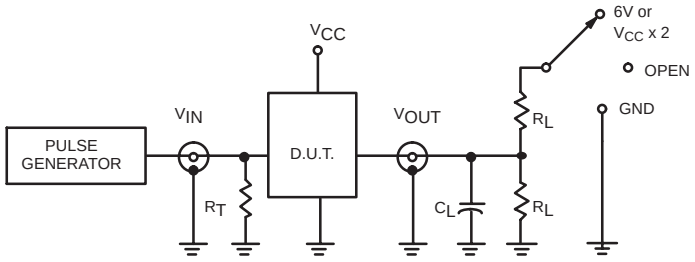


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

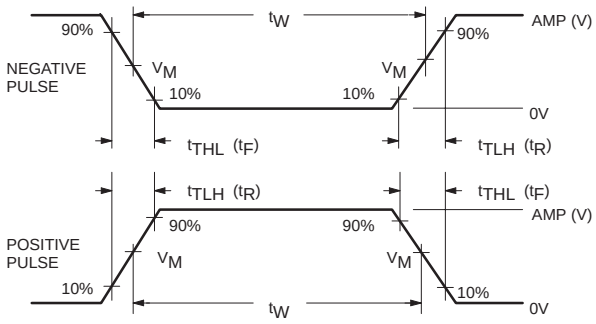


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V or V_{CC} / 2, whichever is less
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

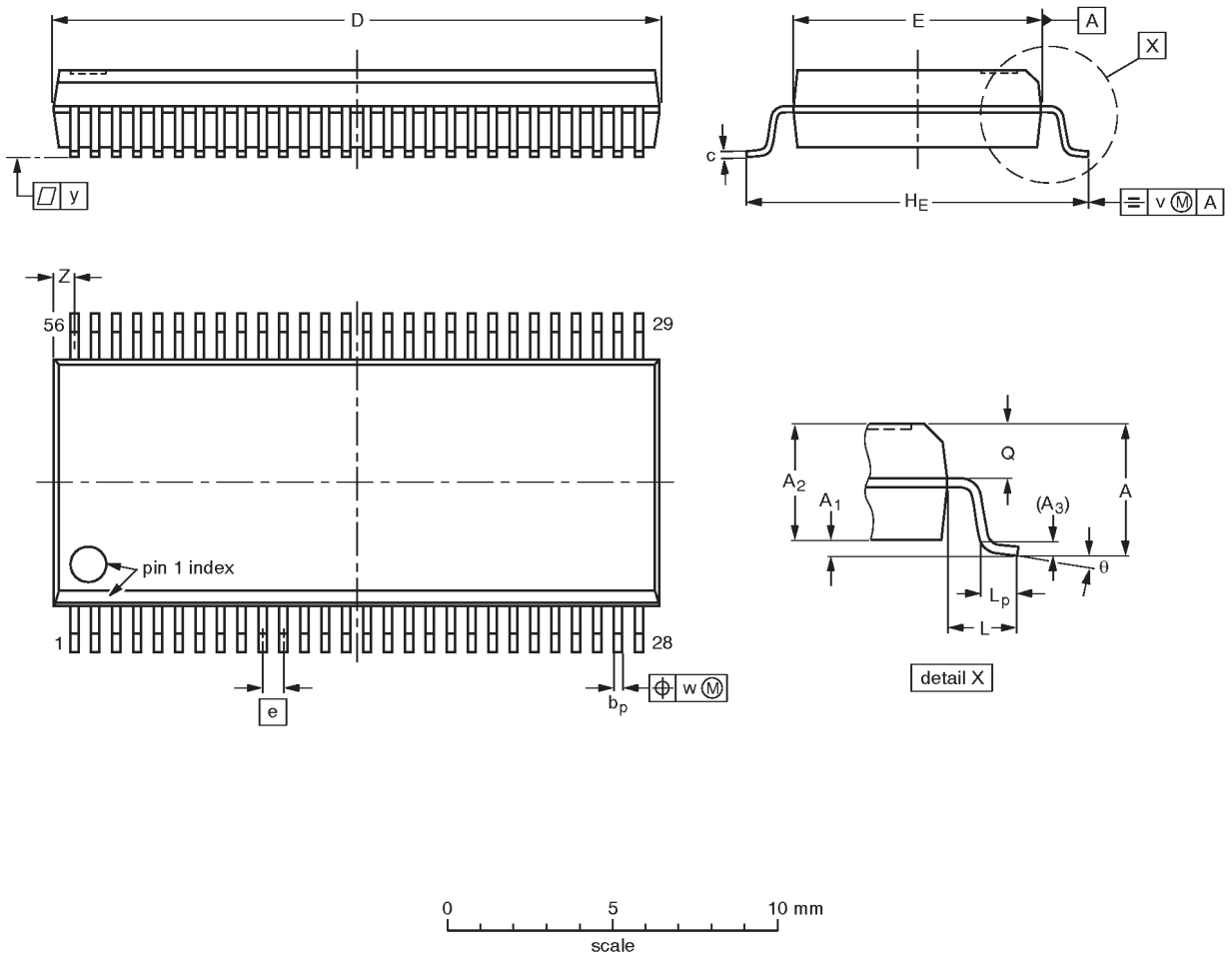
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00162

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

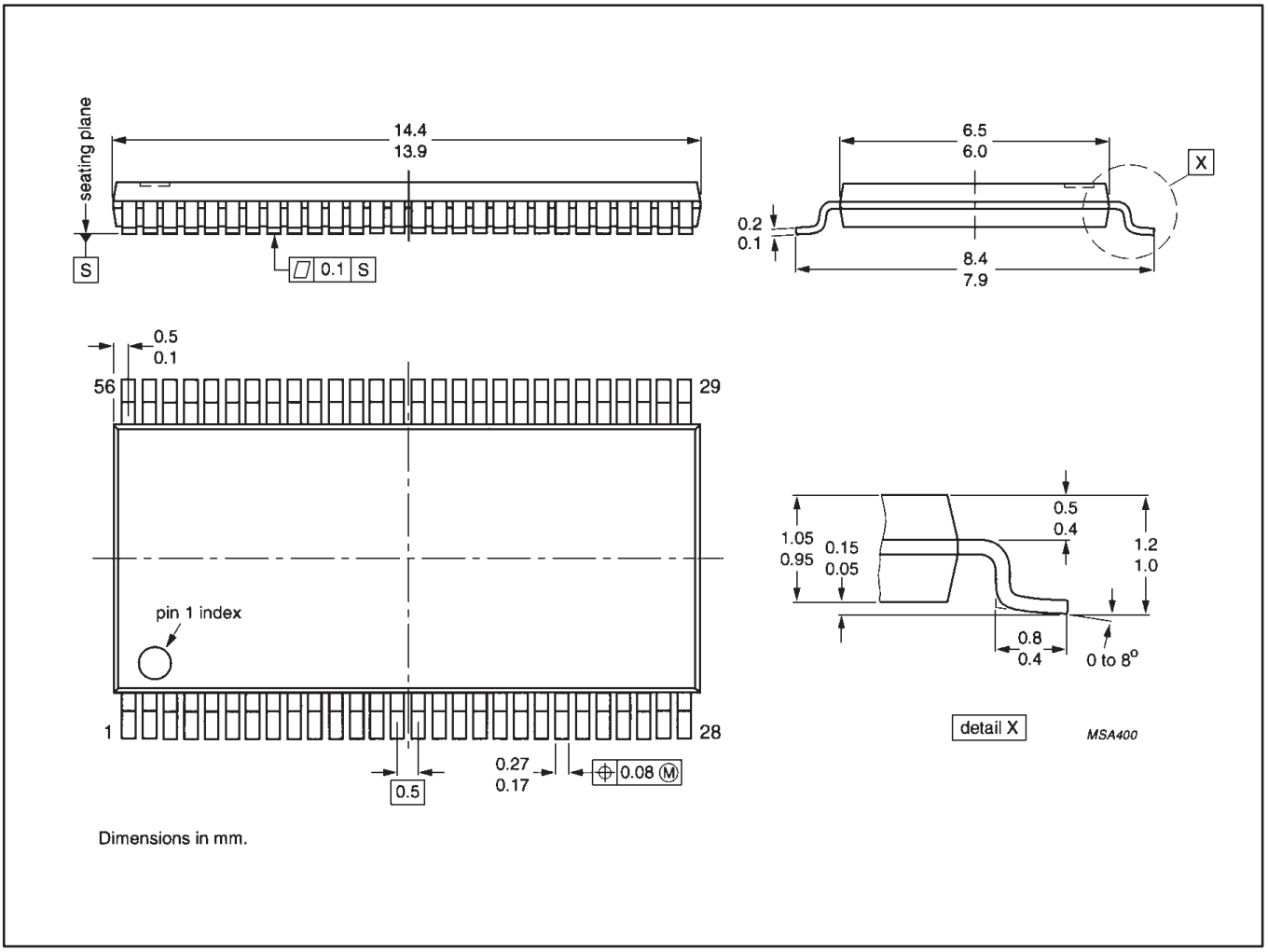
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



Dimensions in mm.

NOTES

18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

74ALVT162823

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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